Lanai Z8ES

Programmable, Dual-Port, 10Gb / PCI Express Controller

Datasheet

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All specifications presented in this document are subject to change at any time, and without prior notice.

Revision Log

Rev.	Date	Changes/Additions
1.0	14 Oct 2008	
1.1	7 Nov 2008	- Dropped parallel-EEPROM support. - Added SMBC/SMBD/PWAKEb leakage-current Erratum (page 20).
1.2	12 Aug 2009	- PLL_TEST pin renamed to PLL_RSTb - Modified Power Sequencing section 3.6. - Modified recommended loopback control in dual-CX4 configuration fig. 3-12. - Minimum EEPROM size changed to 1024Kx8 in section 3.11

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1 INTRODUCTION

1.1 Functional Description

The Myricom Lanai Z8ES is a single-chip, low-power, wire-rate-performance, dual-port, 10Gb/s network controller for PCI Express (PCIe) applications.

- The host port is a native 8-lane (x8) PCIe 2.0 compliant interface (2.5 GT/s only), qualified with all leading PCIe chipsets and all major operating systems.

- The network ports are XAUI (per IEEE 802.3ae) at the Physical (PHY) level, and can be configured to operate in either 10-Gigabit Ethernet or 10-Gigabit Myrinet mode at the Data Link level.

The previous version of this chip, Lanai Z8E, has been shipping in highly successful PCIe network-interface cards (NICs) since December 2005. The Lanai Z8ES differs from the Lanai Z8E in integrating the high-speed SRAM within the chip, in adding a second 10Gb/s network port for failover, in operating at a higher clock rate and at lower power, in supporting PCIe Single-Root IO Virtualization (SR-IOV), and in many other improvements.

In addition to a RISC processor and 2MB of high-speed SRAM, the Lanai Z8ES contains a set of packet engines that handle the packet payloads at wire rate. Firmware executing in the RISC handles the packet headers, and controls the actions of the packet engines. For Ethernet operation, the firmware/hardware combination implements all important stateless TCP/IP and UDP/IP offloads. Optional firmware may be used to support low-latency kernel-bypass operation for High Performance Computing, Video, or other demanding applications.

1.2 Lanai Z8ES Features

•Low Power, Small System Footprint

- 2.2W typical (2.5W maximum) power consumption at nominal CPU frequency of 338.5MHz
- 25mm square, 316-pin, flip-chip BGA (FCBGA) package
- Requires only two active external components: 156.25MHz reference clock, and a serial EEPROM

•PCI Express Interface

- PCI Express x8 interface, PCIe 2.0 compliant (2.5 GT/s only)
- PCIe data transfer rates with all leading PCIe chipsets are greater than 12Gb/s unidirectional and 22 Gb/s bidirectional (see http://www.myri.com/scs/performance/PCIe_motherboards)
- Able to negotiate down to and operate in x4, x2, or x1 mode
- Supports optional low-swing transmitter output levels, and transmitter margining
- Supports legacy interrupts (INTx), as well as MSI and MSI-X interrupts
- Supports issuing of up to 16 outstanding Read requests
- Supports up to 4KB MaxPayloadSize for all packet types
- Optional Advanced Error Reporting supported
- Optional Completion Timeout Control supported
- Address Translation Services, Rev. 1.0 compliant
- Single Root I/O Virtualization and Sharing Specification, Rev. 1.0 compliant
- Optional Alternative Routing-ID Interpretation (ARI) supported
- Optional Function Level Reset (FLR) supported
- Optional System Management Bus (SMBus) supported

•10Gb/s Network Ports

- Two network ports, each configurable in either 10G Ethernet (per IEEE 802.3ae) or 10G Myrinet mode. Two ports are provided for fail-over support.
- Integrated XAUI and MDC/MDIO interfaces support the full range of 10GBASE-X, 10GBASE-R, 10GBASE-W, and 10GBASE-T PHY devices, as well as any other 10-Gigabit Ethernet PHYs that may be defined in the future
- Hardware capable of line-rate unidirectional and bidirectional performance for all Ethernet packet sizes; the actual in-system small-packet performance is typically limited by the host networking stack (see http://www.myri.com/scs/performance)
- Hardware flow-control implementation in both Ethernet and Myrinet mode
- Hardware capable of data-rate throttling to 9.58464 Gb/s, as required for 10GBASE-W, and Inter-Packet Gap stretching
- Full hardware support for two MAC addresses, one per network port. The hardware for each port can span up to 256 contiguous MAC addresses. For applications requiring large numbers of non-contiguous MAC addresses, firmware (with hardware hash assist) can efficiently support up to 1024 unicast or multicast MAC addresses.

•Reliability, Availability, and Serviceability (RAS) features

- Extensive set of self-test features and loopback modes
- Parity protection of all on-chip memories
- Self-reboot and self-reinitialization upon detected hardware or firmware faults, without bringing down the PCIe link

•Software- and Firmware-Development Support

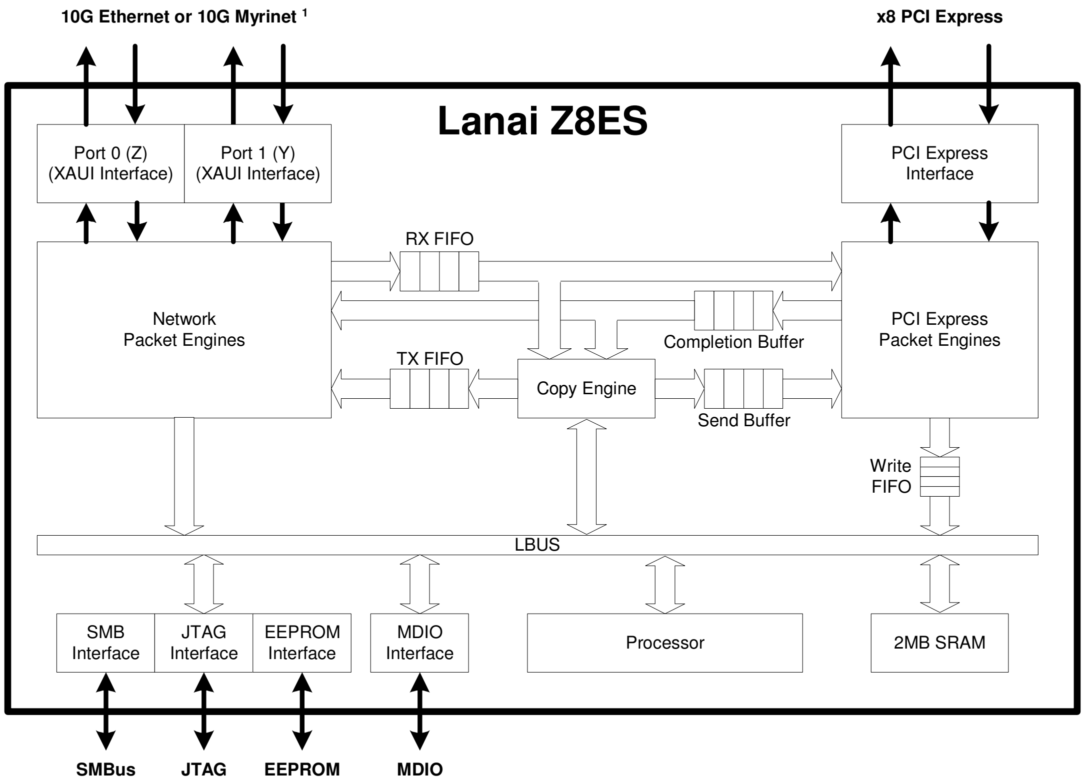
- Mature open-source Ethernet device drivers available for the following operating systems:
  - Linux (included in 2.6.18 and later kernels)
  - Windows (WHQL certified)
  - Solaris 10
  - Mac OS X (10.4 and later)
  - FreeBSD (included in FreeBSD 6.3 and later)
  - NetBSD[1]
  - Plan 9[1]
  - VMware ESX
- All major stateless offloads supported, including
  - TCP/IP and UDP/IP checksum offloading for Tx and Rx, IPv4 and IPv6
  - TCP Segmentation Offload (TSO), also referred to Large Send Offload (LSO)
  - Large Receive Offload (LRO)
  - Receive Side Scaling (RSS)[2]
  - Interrupt coalescing
  - Multiple Rx and Tx queues[2]; firmware-driven, hardware-assisted matching for complete flexibility and high performance
- Generally available Ethernet Driver Software Interface manual, the driver-development kit (DDK)
- Customizable EEPROM-image-building utility with standard, Myricom-supplied, 10G Ethernet firmware, including an Etherboot (UEFI- and PXE-compatible) driver
- Open-source Firmware Development Kit (FDK) available with a full set of GNU-based (compiler, linker, loader, libraries, and debugger), and TCL-based (scripting) tools. The FDK requires an NDA and a non-redistribution agreement.

Note 1: Developed, maintained, and available from non-Myricom sources.
Note 2: These offloads may not be available on all supported operating systems.

1.3 Lanai Z8ES Block Diagram

The Lanai Z8ES block diagram is shown in the following figure.

Figure 1-1: Lanai Z8ES Block Diagram



Note 1: When only one port is required, the Z port should be used.

The processor, SRAM, and packet engines operate from a common clock at 312.5MHz (lowest power), 338.5MHz (nominal), or 364.6MHz (highest performance) depending on the core supply voltage.

1.4 Related Documentation

- ***Lanai Z8ES EEPROM Configuration Utility*** – In several places in this datasheet we refer to configurable options (such as signal polarity). This utility enables one to produce an EEPROM image with standard, Myricom-supplied, 10G Ethernet firmware, customized to the system application at hand.
- ***Lanai Z8ES Programmer's Reference Guide*** – This document, which is available under an NDA, is required only for customers who are considering writing their own firmware rather than using firmware supplied by Myricom.

1.5 Relevant Standards

The Lanai Z8ES adheres to the following standards:

- IEEE Std 802.3, 2005 Edition,
- IEEE Std 802.3ae, 2002 Edition
- PCI Express Base Specification, Revision 2.0, PCI Express
- PCI Express Card Electromechanical Specification, Revision 2.0
- PCI Bus Power Management Interface Specification, Revision 1.2
- Single Root I/O Virtualization and Sharing Specification, Revision 1.0
- Address Translation Services, Revision 1.0
- PCI Local Bus Specification, Revision 3.0
- PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0
- IEEE Std 1149.1-1990, (JTAG)
- ANSI / VITA 26-1988, (ANSI Myrinet)

2 SIGNAL DESCRIPTIONS

2.1 Pin List By Function

2.1.1 Power Pins

Table 2-1: Power Pins

Name	Pins	Description
Vdd	C4, C6, C8, C10, C12, C14, C16, C18, C20, D22, E3, F22, G3, H22, J3, K22, L3, M22, N3, P22, R3, T22, U3, V22, W3, Y22, AA3, AB5, AB7, AB9, AB11, AB13, AB15, AB17, AB19, AB21	1.2V supply
V25	F24, G1, K24, L1, P24, R1, V24, W1	2.5V supply, digital I/O
GND	A1, A2, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A22, A23, A24, B1, B2, B3, B22, B23, B24, C1, C2, C3, C22, C23, C24, D1, E24, F1, G24, H1, J24, K1, L24, M1, N24, P1, R24, T1, U24, V1, W24, Y1, AA24, AB1, AB2, AB3, AB22, AB23, AB24, AC1, AC2, AC3, AC22, AC23, AC24, AD1, AD2, AD3, AD4, AD6, AD8, AD10, AD12, AD14, AD16, AD18, AD20, AD22, AD23, AD24	Ground
PGND	J9, J10, J11, J12, J13, J14, J15, J16, K9, K10, K11, K12, K13, K14, K15, K16, L9, L10, L11, L12, L13, L14, L15, L16, M9, M10, M11, M12, M13, M14, M15, M16, N9, N10, N11, N12, N13, N14, N15, N16, P9, P10, P11, P12, P13, P14, P15, P16, R9, R10, R11, R12, R13, R14, R15, R16, T9, T10, T11, T12, T13, T14, T15, T16	In addition to electrical ground, these pins provide a thermal path for heat dissipation
AVdd [1]	B4, AC4	Analog 2.5V supply

Note 1: These pins should be filtered with a 15 ohm resistor to V25 and a 1uF capacitor to GND.

2.1.2 Signal-Pin Types

Table 2-2: Signal-Pin Types

Type	Description
I [2]	Regular, 2.5V input pin.
I(XAUI)	XAUI differential input.
I(PCIe)	PCIe differential input.
I(PCIe CLK)	PCIe differential clock input.
O	Regular, 2.5V output pin.
O(1.2V)	1.2V output pin.
O(XAUI)	XAUI differential output.
O(PCIe)	PCIe differential output.
I/O [2]	Regular, 2.5V input/output pin.
I/O(1.2V), OD [2]	1.2V input/output pin, with open-drain output.
I/O(3.3V), OD [1]	3.3V input/output pin, with open-drain output.
A	Analog reference/bias pin.
Qualifier	**Description**
OD	Open drain.
PU	Internal pull-up.
PD	Internal pull-down.

Note 1: These pins are 3.3V-tolerant.
Note 2: These pins are 3.3V-tolerant, but may draw excessive current; if connected to a signal that can exceed 2.5V, add a resistor to limit the current to 10mA.

2.1.3 Clock and Reset Pins

Table 2-3: Clock and Reset Pins

Name	Type	Pin	Description
CLK	I	D2	Reference-clock input, 156.25 MHz, ±100ppm.
RSTb	I	F2	Hardware reset, active-low.
RST2b [1]	I, PU	H2	Software reset, active-low. This pin may optionally be connected to an external reset signal.
PGOOD [1]	I, PD	D3	Power Good. This pin may optionally be connected to a power-good indicator.

Note 1: The only effect of asserting one of these pins is that a corresponding bit in the Lanai status register is set; intended for Wakeup-On-LAN applications. Contact Myricom for details.

2.1.4 PCI Express Pins

Table 2-4: PCI Express Pins

Name	Type	Pin	Description
PRX0p PRX0n	I(PCIe) I(PCIe)	AD5 AC5	Receive differential pair for PCIe lane 0
PRX1p PRX1n	I(PCIe) I(PCIe)	AD7 AC7	Receive differential pair for PCIe lane 1
PRX2p PRX2n	I(PCIe) I(PCIe)	AD9 AC9	Receive differential pair for PCIe lane 2
PRX3p PRX3n	I(PCIe) I(PCIe)	AD11 AC11	Receive differential pair for PCIe lane 3
PRX4p PRX4n	I(PCIe) I(PCIe)	AD13 AC13	Receive differential pair for PCIe lane 4
PRX5p PRX5n	I(PCIe) I(PCIe)	AD15 AC15	Receive differential pair for PCIe lane 5
PRX6p PRX6n	I(PCIe) I(PCIe)	AD17 AC17	Receive differential pair for PCIe lane 6
PRX7p PRX7n	I(PCIe) I(PCIe)	AD19 AC19	Receive differential pair for PCIe lane 7
PTX0p PTX0n	O(PCIe) O(PCIe)	AC6 AB6	Transmit differential pair for PCIe lane 0
PTX1p PTX1n	O(PCIe) O(PCIe)	AC8 AB8	Transmit differential pair for PCIe lane 1
PTX2p PTX2n	O(PCIe) O(PCIe)	AC10 AB10	Transmit differential pair for PCIe lane 2
PTX3p PTX3n	O(PCIe) O(PCIe)	AC12 AB12	Transmit differential pair for PCIe lane 3
PTX4p PTX4n	O(PCIe) O(PCIe)	AC14 AB14	Transmit differential pair for PCIe lane 4
PTX5p PTX5n	O(PCIe) O(PCIe)	AC16 AB16	Transmit differential pair for PCIe lane 5
PTX6p PTX6n	O(PCIe) O(PCIe)	AC18 AB18	Transmit differential pair for PCIe lane 6
PTX7p PTX7n	O(PCIe) O(PCIe)	AC20 AB20	Transmit differential pair for PCIe lane 7
PCLK PCLKb	I(PCIe CLK) I(PCIe CLK)	AA1 AA2	100MHz PCI Express differential reference clock. See page 24 for more information on these signals.
PWAKEb	I/O(3.3V), OD	W2	Wake signal for PCI Express (see Erratum on page 20)
SMBC	I/O(3.3V), OD	Y3	SMBus clock (see Erratum on page 20)
SMBD	I/O(3.3V), OD	Y2	SMBus data (see Erratum on page 20)

2.1.5 XAUI Pins

Table 2-5: XAUI Pins

Name	Type	Pin	Description
YRX0p YRX0n	I(XAUI) I(XAUI)	A14 B14	Receive differential pair 0 for Port Y
YRX1p YRX1n	I(XAUI) I(XAUI)	A16 B16	Receive differential pair 1 for Port Y
YRX2p YRX2n	I(XAUI) I(XAUI)	A18 B18	Receive differential pair 2 for Port Y
YRX3p YRX3n	I(XAUI) I(XAUI)	A20 B20	Receive differential pair 3 for Port Y
YTX0p YTX0n	O(XAUI) O(XAUI)	B13 C13	Transmit differential pair 0 for Port Y
YTX1p YTX1n	O(XAUI) O(XAUI)	B15 C15	Transmit differential pair 1 for Port Y
YTX2p YTX2n	O(XAUI) O(XAUI)	B17 C17	Transmit differential pair 2 for Port Y
YTX3p YTX3n	O(XAUI) O(XAUI)	B19 C19	Transmit differential pair 3 for Port Y
ZRX0p ZRX0n	I(XAUI) I(XAUI)	A6 B6	Receive differential pair 0 for Port Z
ZRX1p ZRX1n	I(XAUI) I(XAUI)	A8 B8	Receive differential pair 1 for Port Z
ZRX2p ZRX2n	I(XAUI) I(XAUI)	A10 B10	Receive differential pair 2 for Port Z
ZRX3p ZRX3n	I(XAUI) I(XAUI)	A12 B12	Receive differential pair 3 for Port Z
ZTX0p ZTX0n	O(XAUI) O(XAUI)	B5 C5	Transmit differential pair 0 for Port Z
ZTX1p ZTX1n	O(XAUI) O(XAUI)	B7 C7	Transmit differential pair 1 for Port Z
ZTX2p ZTX2n	O(XAUI) O(XAUI)	B9 C9	Transmit differential pair 2 for Port Z
ZTX3p ZTX3n	O(XAUI) O(XAUI)	B11 C11	Transmit differential pair 3 for Port Z
VSET0 VSET1	A A	E1 E2	Voltage-output-swing references for XAUI ports. See Section 3.9.1 for details.
ZSIG_DET YSIG_DET	I I	AC21 AD21	Signal-detect inputs controlled by the outputs of PHY devices. The polarity of these signals is configurable.
MDIO MDC	I/O(1.2V), OD I/O(1.2V), OD	B21 C21	General-purpose I/O pins, controlled by the Lanai Z8ES processor, and typically used to implement the Management Data Input/Output Interface per IEEE 802.3, Section 22.2.4.5, and/or IEEE 802.3ae, Section 45.
ZPIN	A	A4	Impedance-adjustment reference. Pin should be left unconnected during normal operation.

Note: When only one port is required, the Z port should be used, and the Y port can be left unconnected.

2.1.6 EEPROM Pins

Table 2-6: EEPROM Pins

Name	Type	Pin	Description
SERMODE	I	U2	EEPROM Mode Select: 0 = Parallel EEPROM (deprecated feature) 1 = Serial EEPROM
SER_DO	I/O	P23	Serial EEPROM data out
SER_CLK	I/O	N22	Serial EEPROM clock
SER_CEb	I/O	N23	Serial EEPROM chip enable
SER_DI	I/O	R23	Serial EEPROM data in
GPI1	I/O	R22	General-purpose input pin (for I^2C)
GPI2	I/O	T24	General-purpose input pin (for I^2C)
GPO1	I/O	W22	General-purpose output pin (for I^2C)
GPO2	I/O	G22	General-purpose output pin (for I^2C)
CPU_FREQ0	I/O	T23	CPU frequency configuration (see Note)
CPU_FREQ1	I/O	U23	CPU frequency configuration
CPU_FREQ2	I/O	U22	CPU frequency configuration
CPU_FREQ3	I/O	V23	CPU frequency configuration
CPU_FREQ4	I/O	W23	CPU frequency configuration

Note: In serial-EEPROM mode, the initial frequency of the CPU clock is set by this pin-strapping option, and equal to 156.25MHz / 6 * CPU_FREQ[4:0]. This setting can be overridden in EEPROM.

2.1.7 LED Pins

Table 2-7: LED Pins

Name	Type	Pin	Description
LED0 [1]	O	G2	LED Output. On Myricom NICs, connects to a yellow, CPU-controlled, firmware-status LED.
LED1 [1]	O		The same as JREQ pin, see Section 2.1.8
LED2 [1]	O	J1	General-purpose output
LED3 [1]	O	J2	General-purpose output
ZLED0 [1, 2, 3] YLED0 [1, 2, 3]	O(1.2V) O(1.2V)	K3 M3	LED Output. In three-LED port configuration, connects to the link-status LED; in single-LED port configuration, asserted when the link status is up, flashes when there is RX or TX activity.
ZLED1 [1, 2] YLED1 [1, 2]	O(1.2V) O(1.2V)	L2 N1	LED Output. In three-LED configuration, connects to the TX-activity LED; unused in single-LED configuration.
ZLED2 [1, 2] YLED2 [1, 2]	O(1.2V) O(1.2V)	M2 N2	LED Output. In three-LED configuration, connects to the RX-activity LED; unused in single-LED configuration.

Note 1: All LED pins are of configurable polarity. Polarity of the LED[3:0] pins can be configured individually, whereas a single bit configures polarity of all ZLED and all YLED pins.
Note 2: A single bit selects three-LED vs. single-LED port configuration for both network ports.
Note 3: When not used to drive port-status LED indicators, connect directly to test points.

2.1.8 Test and Miscellaneous Pins

Table 2-8: Test and Miscellaneous Pins

Name	Type	Pin	Description
TDI	I/O, PD	P2	JTAG Test Data Input
TCK	I/O, PD	U1	JTAG Test Clock
TDO	O	R2	JTAG Test Data Output
TMS	I/O, PU	T2	JTAG Test Mode Select
JMASTER [1]	I, PU	V2	If this pin is high when RSTb is de-asserted, the device will boot from the external EEPROM. Otherwise, no boot load takes place, and the chip remains in an idle state; it can then be booted via the SMBus and/or JTAG interface. Pin should be left unconnected during normal operation.
JWAKEb [1]	I	F3	Level-sensitive negative input. When asserted, it sets a status bit in the Lanai status register.
LBLK	I, PD	P3	Lanai Lockout. This pin blocks Lanai CPU's access to JTAG. Pin should be left unconnected during normal operation.
RPROT	I, PD	T3	EEPROM write protect. Pin should be left unconnected during normal operation.
JREQ [1]	O	H3	JTAG Request output. This pin is also referred to as LED1 (Section 2.1.7).
JOE	I, PU	V3	JTAG Output Enable. When JOE and JMASTER are both asserted, the Lanai chip can drive TCK and TMS to become the master in a daisy chain of JTAG-connected devices.
PLL_RSTb	I, PU	K2	PLL Reset input. Refer to the Power Sequencing section for more information.
D.N.C.		D23, D24, E22, E23, F23, G23, H23, H24, J22, J23, K23, L22, L23, M23, M24, Y23, Y24, AA22, AA23, AB4	Do Not Connect these pins.

Note 1: These pins are used to arbitrate access to the internal JTAG interface between the Lanai CPU on one side, and external JTAG interface and/or SMBus-initiated JTAG access on the other. See Section 3.12 for details.

2.2 Pinout By Pin Order

Table 2-9: Pinout By Pin Order (Part 1)

Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	C1	GND	H1	GND
A2	GND	C2	GND	H2	RST2b
A3	GND	C3	GND	H3	JREQ
A4	ZPIN	C4	Vdd	H22	Vdd
A5	GND	C5	ZTX0n	H23	D.N.C.
A6	ZRX0p	C6	Vdd	H24	D.N.C.
A7	GND	C7	ZTX1n	J1	LED2
A8	ZRX1p	C8	Vdd	J2	LED3
A9	GND	C9	ZTX2n	J3	Vdd
A10	ZRX2p	C10	Vdd	J9	PGND
A11	GND	C11	ZTX3n	J10	PGND
A12	ZRX3p	C12	Vdd	J11	PGND
A13	GND	C13	YTX0n	J12	PGND
A14	YRX0p	C14	Vdd	J13	PGND
A15	GND	C15	YTX1n	J14	PGND
A16	YRX1p	C16	Vdd	J15	PGND
A17	GND	C17	YTX2n	J16	PGND
A18	YRX2p	C18	Vdd	J22	D.N.C.
A19	GND	C19	YTX3n	J23	D.N.C.
A20	YRX3p	C20	Vdd	J24	GND
A21	GND	C21	MDC	K1	GND
A22	GND	C22	GND	K2	PLL_RSTb
A23	GND	C23	GND	K3	ZLED0
A24	GND	C24	GND	K9	PGND
B1	GND	D1	GND	K10	PGND
B2	GND	D2	CLK	K11	PGND
B3	GND	D3	PGOOD	K12	PGND
B4	AVdd	D22	Vdd	K13	PGND
B5	ZTX0p	D23	D.N.C.	K14	PGND
B6	ZRX0n	D24	D.N.C.	K15	PGND
B7	ZTX1p	E1	VSET0	K16	PGND
B8	ZRX1n	E2	VSET1	K22	Vdd
B9	ZTX2p	E3	Vdd	K23	D.N.C.
B10	ZRX2n	E22	D.N.C.	K24	V25
B11	ZTX3p	E23	D.N.C.	L1	V25
B12	ZRX3n	E24	GND	L2	ZLED1
B13	YTX0p	F1	GND	L3	Vdd
B14	YRX0n	F2	RSTb	L9	PGND
B15	YTX1p	F3	JWAKEb	L10	PGND
B16	YRX1n	F22	Vdd	L11	PGND
B17	YTX2p	F23	D.N.C.	L12	PGND
B18	YRX2n	F24	V25	L13	PGND
B19	YTX3p	G1	V25	L14	PGND
B20	YRX3n	G2	LED0	L15	PGND
B21	MDIO	G3	Vdd	L16	PGND
B22	GND	G22	GPO2	L22	D.N.C.
B23	GND	G23	D.N.C.	L23	D.N.C.
B24	GND	G24	GND	L24	GND

Table 2-10: Pinout By Pin Order (Part 2)

Pin	Signal	Pin	Signal	Pin	Signal
M1	GND	R15	PGND	AB3	GND
M2	ZLED2	R16	PGND	AB4	D.N.C.
M3	YLED0	R22	GPI1	AB5	Vdd
M9	PGND	R23	SER_DI	AB6	PTX0n
M10	PGND	R24	GND	AB7	Vdd
M11	PGND	T1	GND	AB8	PTX1n
M12	PGND	T2	TMS	AB9	Vdd
M13	PGND	T3	RPROT	AB10	PTX2n
M14	PGND	T9	PGND	AB11	Vdd
M15	PGND	T10	PGND	AB12	PTX3n
M16	PGND	T11	PGND	AB13	Vdd
M22	Vdd	T12	PGND	AB14	PTX4n
M23	D.N.C.	T13	PGND	AB15	Vdd
M24	D.N.C.	T14	PGND	AB16	PTX5n
N1	YLED1	T15	PGND	AB17	Vdd
N2	YLED2	T16	PGND	AB18	PTX6n
N3	Vdd	T22	Vdd	AB19	Vdd
N9	PGND	T23	CPU_FREQ0	AB20	PTX7n
N10	PGND	T24	GPI2	AB21	Vdd
N11	PGND	U1	TCK	AB22	GND
N12	PGND	U2	SERMODE	AB23	GND
N13	PGND	U3	Vdd	AB24	GND
N14	PGND	U22	CPU_FREQ2	AC1	GND
N15	PGND	U23	CPU_FREQ1	AC2	GND
N16	PGND	U24	GND	AC3	GND
N22	SER_CLK	V1	GND	AC4	AVdd
N23	SER_CEb	V2	JMASTER	AC5	PRX0n
N24	GND	V3	JOE	AC6	PTX0p
P1	GND	V22	Vdd	AC7	PRX1n
P2	TDI	V23	CPU_FREQ3	AC8	PTX1p
P3	LBLK	V24	V25	AC9	PRX2n
P9	PGND	W1	V25	AC10	PTX2p
P10	PGND	W2	PWAKEb	AC11	PRX3n
P11	PGND	W3	Vdd	AC12	PTX3p
P12	PGND	W22	GPO1	AC13	PRX4n
P13	PGND	W23	CPU_FREQ4	AC14	PTX4p
P14	PGND	W24	GND	AC15	PRX5n
P15	PGND	Y1	GND	AC16	PTX5p
P16	PGND	Y2	SMBD	AC17	PRX6n
P22	Vdd	Y3	SMBC	AC18	PTX6p
P23	SER_DO	Y22	Vdd	AC19	PRX7n
P24	V25	Y23	D.N.C.	AC20	PTX7p
R1	V25	Y24	D.N.C.	AC21	ZSIG_DET
R2	TDO	AA1	PCLK	AC22	GND
R3	Vdd	AA2	PCLKb	AC23	GND
R9	PGND	AA3	Vdd	AC24	GND
R10	PGND	AA22	D.N.C.	AD1	GND
R11	PGND	AA23	D.N.C.	AD2	GND
R12	PGND	AA24	GND	AD3	GND
R13	PGND	AB1	GND	AD4	GND
R14	PGND	AB2	GND	AD5	PRX0p

Table 2-11: Pinout By Pin Order (Part 3)

Pin	Signal	Pin	Signal	Pin	Signal
AD6	GND				
AD7	PRX1p				
AD8	GND				
AD9	PRX2p				
AD10	GND				
AD11	PRX3p				
AD12	GND				
AD13	PRX4p				
AD14	GND				
AD15	PRX5p				
AD16	GND				
AD17	PRX6p				
AD18	GND				
AD19	PRX7p				
AD20	GND				
AD21	YSIG_DET				
AD22	GND				
AD23	GND				
AD24	GND				

2.3 Pinout Diagram

Figure 2-1: Pinout Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	GND	GND	GND	ZPIN	GND	ZRX0p	GND	ZRX1p	GND	ZRX2p	GND	ZRX3p	GND	YRX0p	GND	YRX1p	GND	YRX2p	GND	YRX3p	GND	GND	GND	GND
B	GND	GND	GND	AVdd	ZTX0p	ZRX0n	ZTX1p	ZRX1n	ZTX2p	ZRX2n	ZTX3p	ZRX3n	YTX0p	YRX0n	YTX1p	YRX1n	YTX2p	YRX2n	YTX3p	YRX3n	MDIO	GND	GND	GND
C	GND	GND	GND	Vdd	ZTX0n	Vdd	ZTX1n	Vdd	ZTX2n	Vdd	ZTX3n	Vdd	YTX0n	Vdd	YTX1n	Vdd	YTX2n	Vdd	YTX3n	Vdd	MDC	GND	GND	GND
D	GND	CLK	PGOOD																			Vdd	D.N.C.	D.N.C.
E	VSET0	VSET1	Vdd																			D.N.C.	D.N.C.	GND
F	GND	RSTb	JWAKEb																			Vdd	D.N.C.	V25
G	V25	LED0	Vdd																			GPO2	D.N.C.	GND
H	GND	RST2b	JREQ																			Vdd	D.N.C.	D.N.C.
J	LED2	LED3	Vdd						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						D.N.C.	D.N.C.	GND
K	GND	PLL_RSTb	ZLED0						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						Vdd	D.N.C.	V25
L	V25	ZLED1	Vdd						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						D.N.C.	D.N.C.	GND
M	GND	ZLED2	YLED0						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						Vdd	D.N.C.	D.N.C.
N	YLED1	YLED2	Vdd						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						SER_CLK	SER_CEb	GND
P	GND	TDI	LBLK						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						Vdd	SER_DO	V25
R	V25	TDO	Vdd						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						GPI1	SER_DI	GND
T	GND	TMS	RPROT						PGND	PGND	PGND	PGND	PGND	PGND	PGND	PGND						Vdd	CPU_FREQ0	GPI2
U	TCK	SER_MODE	Vdd																			CPU_FREQ2	CPU_FREQ1	GND
V	GND	JMASTER	JOE																			Vdd	CPU_FREQ3	V25
W	V25	PWAKEb	Vdd																			GPO1	CPU_FREQ4	GND
Y	GND	SMBD	SMBC																			Vdd	D.N.C.	D.N.C.
AA	PCLK	PCLKb	Vdd																			D.N.C.	D.N.C.	GND
AB	GND	GND	GND	D.N.C.	Vdd	PTX0n	Vdd	PTX1n	Vdd	PTX2n	Vdd	PTX3n	Vdd	PTX4n	Vdd	PTX5n	Vdd	PTX6n	Vdd	PTX7n	Vdd	GND	GND	GND
AC	GND	GND	GND	AVdd	PRX0n	PTX0p	PRX1n	PTX1p	PRX2n	PTX2p	PRX3n	PTX3p	PRX4n	PTX4p	PRX5n	PTX5p	PRX6n	PTX6p	PRX7n	PTX7p	ZSIG_DET	GND	GND	GND
AD	GND	GND	GND	GND	PRX0p	GND	PRX1p	GND	PRX2p	GND	PRX3p	GND	PRX4p	GND	PRX5p	GND	PRX6p	GND	PRX7p	GND	YSIG_DET	GND	GND	GND

3 Electrical and Timing Specifications

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings [1]

Symbol	Parameter	Min	Max	Unit
V_{DD}	Core Supply Voltage (Vdd pins)	-0.5	+1.4	V
$V_{I/O}$	I/O Supply Voltage (V25 pins)	-0.5	+2.9	V
AV_{DD}	Analog DC Power Supply Voltage (AVdd pins)	-0.5	+2.9	V
V_{IN} / V_{OUT}	Input/Output Voltage (non-3.3V-tolerant pins)	-0.5	$V_{I/O}$ + 0.5	V
	Input/Output Voltage (3.3V-tolerant pins)	-0.5	3.8	V
	Input/Output Voltage (I(XAUI) and I(PCIe) pins)	V_{DD} – 1.0	V_{DD} + 0.5	V
	Input/Output Voltage (I(PCIe CLK) pins)	-0.5	$V_{I/O}$ + 0.5	V
I_{OUT}	DC Output Current		50	mA
I_{IN}	DC Input-Pin Current [2]		15	mA
T_{STOR}	Storage Temperature	-55	150	°C
T_{BIAS}	Junction Temperature Under Bias	-55	125	°C

Note 1: Maximum ratings are referenced to ground (GND). Device damage may occur if ratings provided in the above table are exceeded.

Note 2: The I, I/O, and I/O (1.2V) pins (Section 2.1.2) are 3.3V-tolerant, but may draw excessive current when connected to signals that exceed 2.5V.

3.2 Recommended Operating Conditions

Table 3-2: Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Core Supply Voltage	312.5MHz	1.14	1.20	1.26	V
		338.5MHz	1.20	1.23	1.26	V
		364.6MHz	1.26	1.29	1.32	V
$V_{I/O}$	I/O Supply Voltage		2.375	2.5	2.625	V
AV_{DD}	Analog Power Supply Voltage		2.375	2.5	2.625	V
T_{CASE}	Top-of-Case Temperature		0		90	°C

3.3 Power Specifications

Table 3-3: Power Specifications

Symbol	Parameter		Typ	Max	Unit
I_{DD}	Core Supply Current	312.5MHz	1.55	1.7	A
		338.5MHz	1.65	1.8	A
		364.6MHz	1.80	2.0	A
$I_{I/O}$	I/O Supply Current		50	60	mA
P_{TOT}	Total Power Dissipation	312.5MHz	2.0	2.3	W
		338.5MHz	2.2	2.5	W
		364.6MHz	2.4	2.8	W

3.4 DC Characteristics

Table 3-4: DC Characteristics

Pin Type	Symbol	Parameter	Min	Max	Unit
All	C_I	Input Capacitance		5	pF
	$C_{I/O}$	I/O Capacitance		7	pF
	I_{LI}	Input Leakage Current		± 5	µA
	I_{LO}	Output Leakage Current		± 5	µA
	R_{UP} / R_{DN}	Internal Pull-Up/Pull-Down Resistance	10	30	KΩ
I [2]	V_{IL}	Input Low Threshold	0.8		V
	V_{IH}	Input High Threshold		1.6	V
O	V_{OL} (I_{OL} = 5mA)	Output Low Voltage		0.4	V
	V_{OH} (I_{OH} = -5mA)	Output High Voltage	2.0		V
O(1.2V)	V_{OL} (I_{OL} = 20mA)	Output Low Voltage		0.3	V
	V_{OH} (I_{OH} = -10mA)	Output High Voltage	V_{DD} – 0.2		V
I/O [2]	V_{IL}	Input Low Threshold	0.8		V
	V_{IH}	Input High Threshold		1.6	V
	V_{OL} (I_{OL} = 5mA)	Output Low Voltage		0.4	V
	V_{OH} (I_{OH} = -5mA)	Output High Voltage	2.0		V
I/O(1.2V), OD [2]	V_{IL}	Input Low Threshold	0.4		V
	V_{IH}	Input High Threshold		0.8	V
	V_{OL} (I_{OL} = 5mA)	Output Low Voltage		0.3	V
I/O(3.3V), OD [1]	V_{IL}	Input Low Threshold	0.8		V
	V_{IH}	Input High Threshold		1.6	V
	V_{OL} (I_{OL} = 5mA)	Output Low Voltage		0.3	V
	V_{HYST}	Voltage Hysteresis	0.3		V
	I_{LI} (V_{IH} = 3.3V, Vdd = V25 = 0V)	Input Leakage Current [3]		10	µA

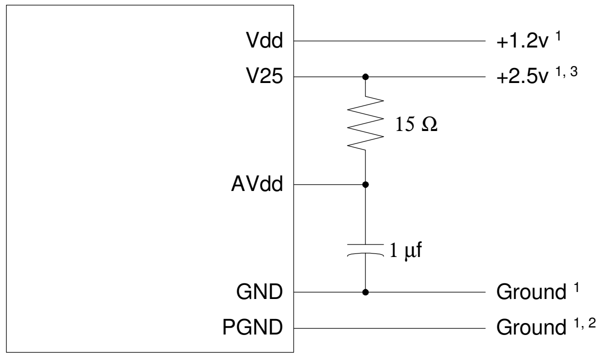
Note 1: These pins are 3.3V-tolerant.

Note 2: These pins are 3.3V-tolerant, but may draw excessive current; if connected to a signal that can exceed 2.5V, add a resistor to limit the current to 10mA.

Note 3: **Erratum:** Leakage current may be up to 250µA at 3.3V, in excess of SMBus (SMBDAT and SMBCLK) and PCI Express (WAKE#) specification. A bus switch such as Texas Instruments SN74CB3T3306 may be used to achieve leakage-current compliance.

3.5 Power Supply Connections

Figure 3-1: Power Supply Connections



Note: 1	Vdd and GND should be carried on plane layers. Although it is not necessary to carry V25 on a plane layer, decoupling near package pins is recommended.
Note: 2	In addtion to serving as ground pins, these pins also provide a thermal path for heat dissipation.
Note: 3	Refer to section 3.6 for power sequencing requirements

Distribute power and decouple as needed.

3.6 Power Sequencing

Figure 3-2: Power Sequencing

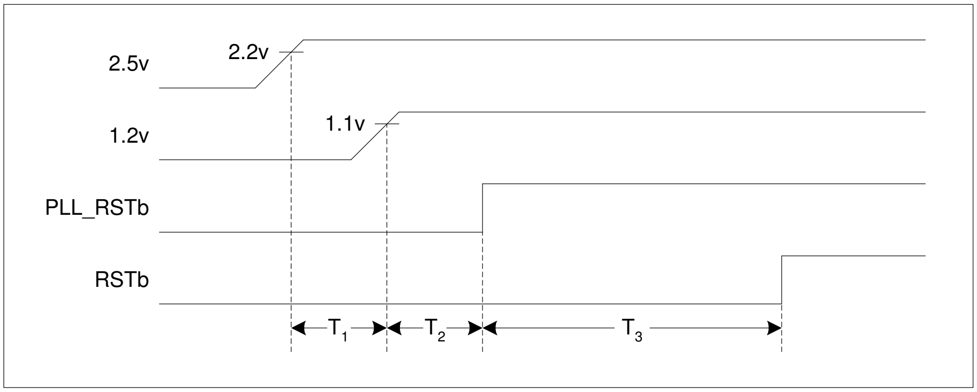


Table 3-5: Power Sequencing Timing Specifications

Parameter	Description	Min
T_1	2.5v present to 1.2v present *	0 ms
T_2	1.2v present to PLL_RSTb	1 ms
T_3	PLL_RSTb to RSTb	10 ms

* Note: Ideally, the 2.5v and 1.2v supplies should ramp up together (T1 = 0), with the 2.5v supply being roughly twice the 1.2v supply during ramp-up. If this is not possible, the 1.2v supply must come up after the 2.5v supply (T1 > 0). During T1, the chip may draw excessive current, up to 1A from the 2.5v supply. The 2.5v supply must be able to maintain at least 2.2v during this time.

3.7 Clock Specification

Figure 3-3: Clock Timing

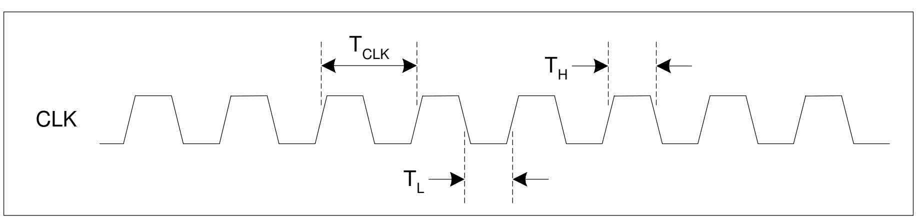


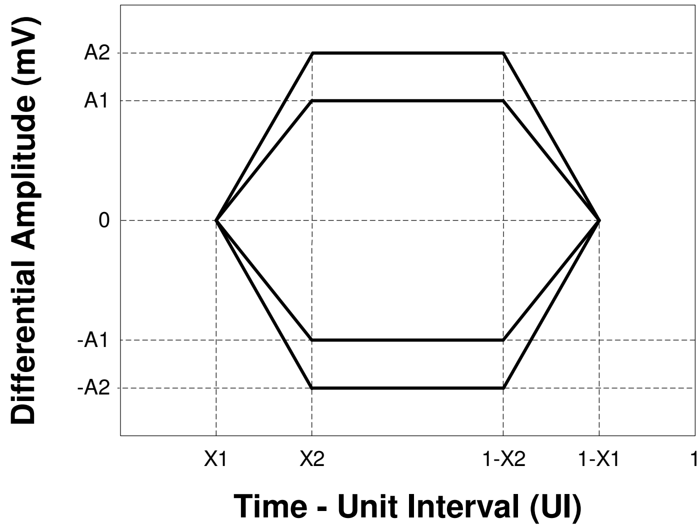
Table 3-6: CLK Timing Specifications

Parameter	Description	Min	Typ	Max
$f_{CLK} = 1/T_{CLK}$	CLK Frequency	156.25 MHz – 100ppm	156.25 MHz	156.25 MHz + 100ppm
T_L	CLK Low Phase	2.56 ns	3.20 ns	3.84 ns
T_H	CLK High Phase	2.56 ns	3.20 ns	3.84 ns
f_J	CLK Frequency Jitter			2ps RMS 12kHz – 20kHz

3.8 PCI Express Interface Specification

3.8.1 Transmitter Output Specifications

Figure 3-4: PCI Express Transmit Eye Diagram



Note: The Differential Amplitude in the above figure is defined as (D+ - D-).

Table 3-7: PCI Express Transmit Specifications

Symbol	Parameter	Near End	Far End	Unit
X1	pTXp – pTXn Crossing Point	0.125 (max)	0.3	UI
X2	pTXp, pTXn Stable	0.5	0.5	UI
A1	De-Emphasized Bit Level	See Note 1	175 (min)	mV
A2	Emphasized Bit Level	400 (min)	175 (min)	mV

Note 1: At the near end, A1 must be between -3.0 and -4.0 dB of A2.

Table 3-8: PCI Express Transmitter Output Specifications

Parameter	Min	Typ	Max	Units
Unit Interval (UI)	399.88	400	400.12	ps
Differential Peak to Peak Amplitude (2*A2)	800		1000	mV
De-Emphasized Output Voltage (Ratio)	3		4	dB
Minimum TX Eye Width (1 – 2*X1)	0.75			UI
D+ / D- TX Output Rise / Fall Time	50		100	ps
RMS AC Peak Common Mode Output Voltage			20	mV
Absolute Delta of DC Common Mode Voltage between D+ and D-			25	mV
Electrical Idle Differential Peak Output Voltage			20	mV
Voltage change allowed during receiver detection			600	mV
Differential Return Loss	12			dB
Common Mode Return Loss	6			dB
DC Differential TX Impedance	80	100	120	Ω
Lane to Lane Output Skew			1	ns

Note 1: The above table does not include spread spectrum.
Note 2: The above table shows output voltage in full-swing mode. The low-swing output and transmitter margining are supported via EEPROM-based configuration.

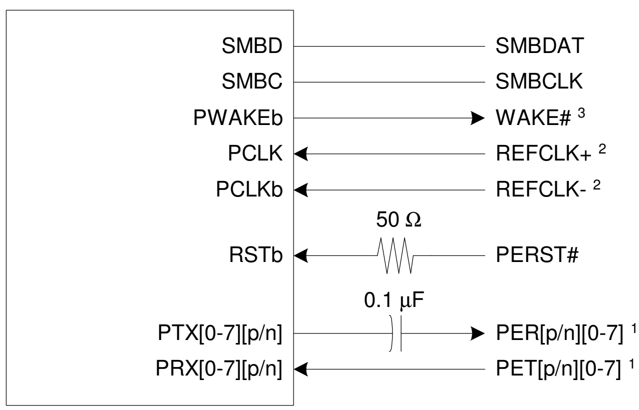
Receiver Input Specifications

Table 3-9: PCI Express Receiver Input Specifications

Parameter	Min	Typ	Max	Units
Unit Interval (UI)	399.88	400	400.12	ps
Differential Peak to Peak Input Voltage (2*A2)	0.175		1.2	V
Minimum RX Eye Width	0.4			UI
AC Peak Common Mode Input Voltage			150	mV
Differential Return Loss	15			dB
Common Mode Return Loss	6			dB
DC Differential Input Impedance	80	100	120	Ω
Total Lane-to-Lane Skew			20	ns

3.8.2 PCIe Interface Diagram

Figure 3-5: PCIe and SMBus Interface Diagram



Note 1: The PTX and PRX lane order must be preserved, but the p and n in each pair may be reversed to ease wiring constraints since PCI Express requires automatic polarity detection and correction.

Note 2: No jitter attenuator is needed for the PCIe reference clock.

Note 3: For typical 10G Ethernet applications, which do not implement Wakeup On LAN, leave PWAKEb unconnected.

3.9 XAUI Interface Specification

3.9.1 XAUI Output-Voltage-Swing Adjustment

The VSET0 and VSET1 pins are used to set the voltage swing of XAUI TX outputs. Each port can be configured to use either of the two voltage references.

If the TX outputs are AC-coupled, the voltage swing is equal to (V_{DD} - VSET). Typically, a VSET is set by a resistor divider to 0.75V, yielding an output swing of approximately 450 mV. A short link may want to set a VSET to higher voltage, reducing the output swing and saving power. On DC-coupled interfaces, the output swing is equal to 2 * (V_{DD} - VSET).

A port can be put in low-power mode, with its output drivers turned off. This is achieved by setting a voltage reference to V_{DD}, and configuring the port to use that voltage reference. It is recommended that VSET1 be used for this purpose.

3.9.2 XAUI Switching Specification

Figure 3-6: XAUI Switching Waveform

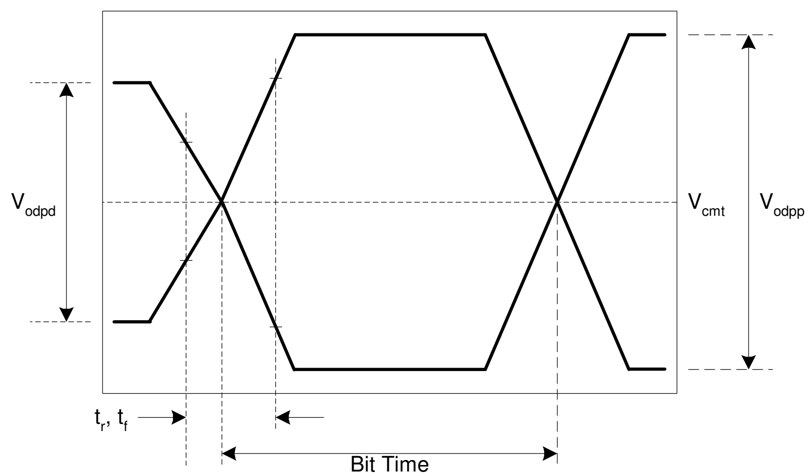


Table 3-10: XAUI Switching Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{odpp}	Differential Peak to Peak Voltage Swing (Emphasized bit)	350	375	400	mV
V_{odpd}	Differential Peak to Peak Voltage Swing (De-Emphasized bit)	230	250	270	mV
t_r, t_f	Differential output signal rise, fall time (20% to 80%)			100	ps
	Receiver Sensitivity	100			mV

3.9.3 XAUI Transmit Specifications

Figure 3-7: XAUI Transmit Eye Diagram

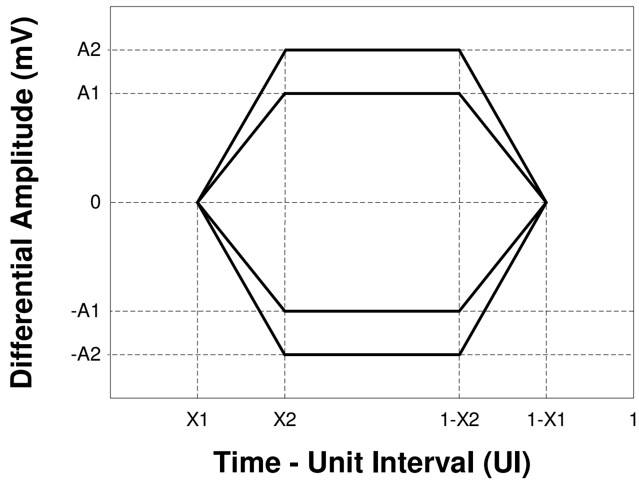


Table 3-11: XAUI Transmit Specifications

Symbol	Parameter	Near End	Far End	Unit
X1	zTXp – zTXn Crossing Point	175	275	mUI
X2	xTXp, zTXn Stable	390	400	mUI
A1	De-Emphasized Bit Level	400	100 (min)	mV
A2	Emphasized Bit Level	450 (min)	450 (min)	mV

3.9.4 XAUI Receive Specifications

Figure 3-8: XAUI Receive Eye Diagram

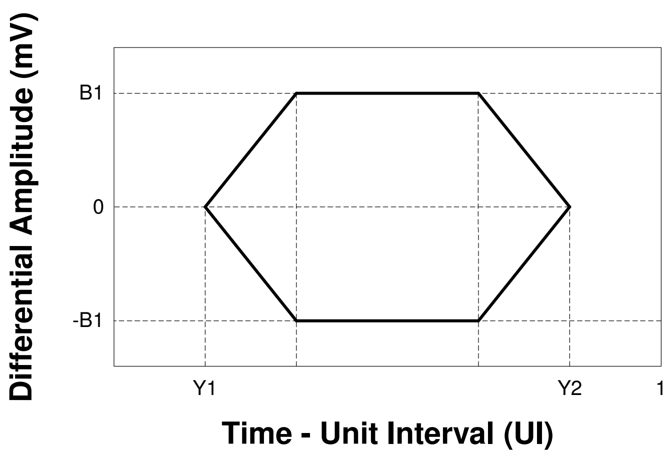


Table 3-12: XAUI Receive Specifications

Symbol	Parameter	Min	Max	Unit
Y1	zRXp – zRXn Crossing Point 1		275	mUI
Y2	zRXp, zRXn Crossing Point 2	625	725	mUI
B1	Bit Level	100		mV

3.9.5 XAUI Jitter Specifications

Figure 3-9: XAUI Jitter Diagram

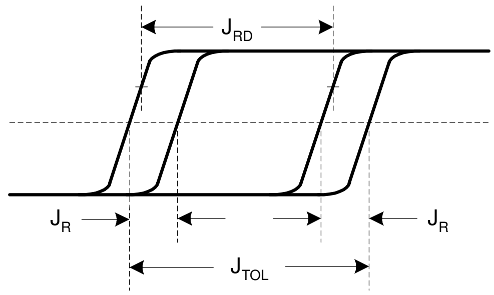
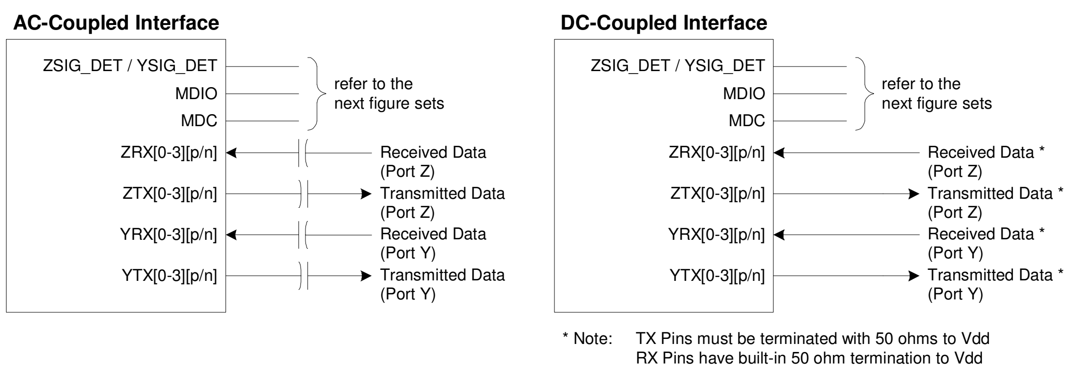


Table 3-13: XAUI Jitter Specifications

Symbol	Parameter	Min	Typ	Max	Units
J_{TOL}	Jitter Tolerance ($J_{TOL} = J_{RD} + J_R$)			0.65	UI
J_{RD}	Received Deterministic Jitter			0.37	UI

3.9.6 XAUI Interface Diagrams

Figure 3-10: XAUI Interface Diagram



Assuming a port is configured to use $VSET_I$ (see Section 3.9.13.9), on an AC-coupled interface the output swing will be equal to (V_{DD} - $VSET_I$), and on a DC-coupled interface the output swing will be equal to 2 * (V_{DD} - $VSET_I$).

In both interfaces, the ZTX and ZRX lane order must be preserved, but the p and n in each pair may be reversed to ease wiring constraints. However, the p/n reversal is not automatic and must be accompanied by a change in configuration.

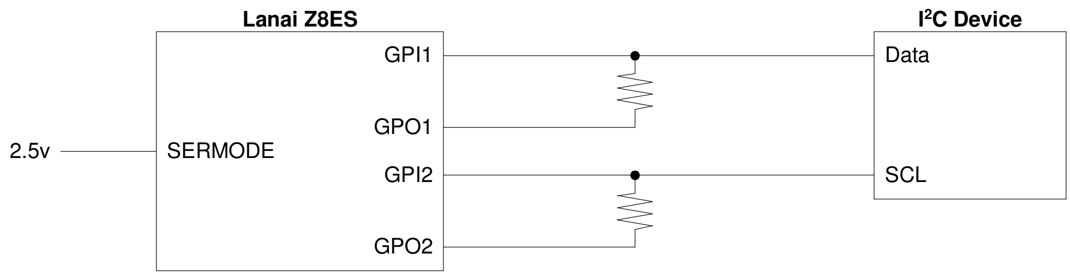
When only one port is required, the Z port should be used, and the Y port can be left unconnected.

3.10 MDIO and I²C Interfaces

MDC and MDIO are general-purpose, open-drain I/O pins, controlled by the Lanai Z8ES processor. They are typically used to implement the Management Data Input/Output Interface per IEEE 802.3, Section 22.2.4.5, and/or IEEE 802.3ae, Section 45. The pins' input thresholds are designed for 1.2V operation, and compliant with the latter standard; they are 3.3V-tolerant. When the pins are not used, they may be left unconnected.

The GPI/GPO pins can be used to implement a secondary SMBus/I²C interface, intended for use only as a bus master to simple SMBus/I²C devices, as illustrated below. When the pins are not used, they may be left unconnected.

Figure 3-11: Secondary SMBus / I²C Interface Diagram



The following examples illustrate common practice on Myricom dual-port NICs. Although not required, following these examples is recommended for compatibility with Myricom-supplied firmware. Single-port configurations use XAUI port Z, and GPI1/GPO1. The MDIO and I²C connections in these examples are not generally applicable; extended voltage-level tolerances of the components used are relied upon.

Figure 3-12: MDIO and I²C Interface Connections in a Dual-CX4 Configuration

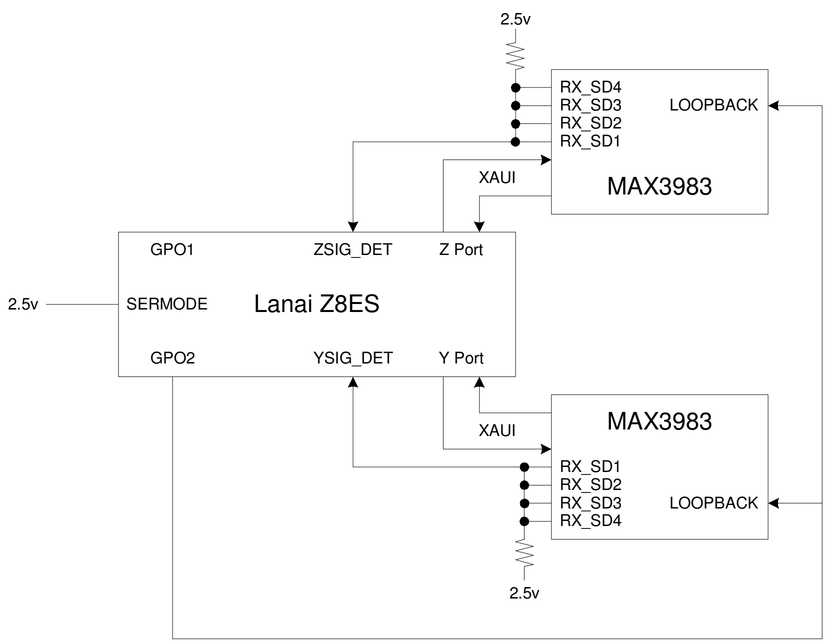


Figure 3-13: MDIO and I²C Interface Connections in a Dual-QSFP Configuration

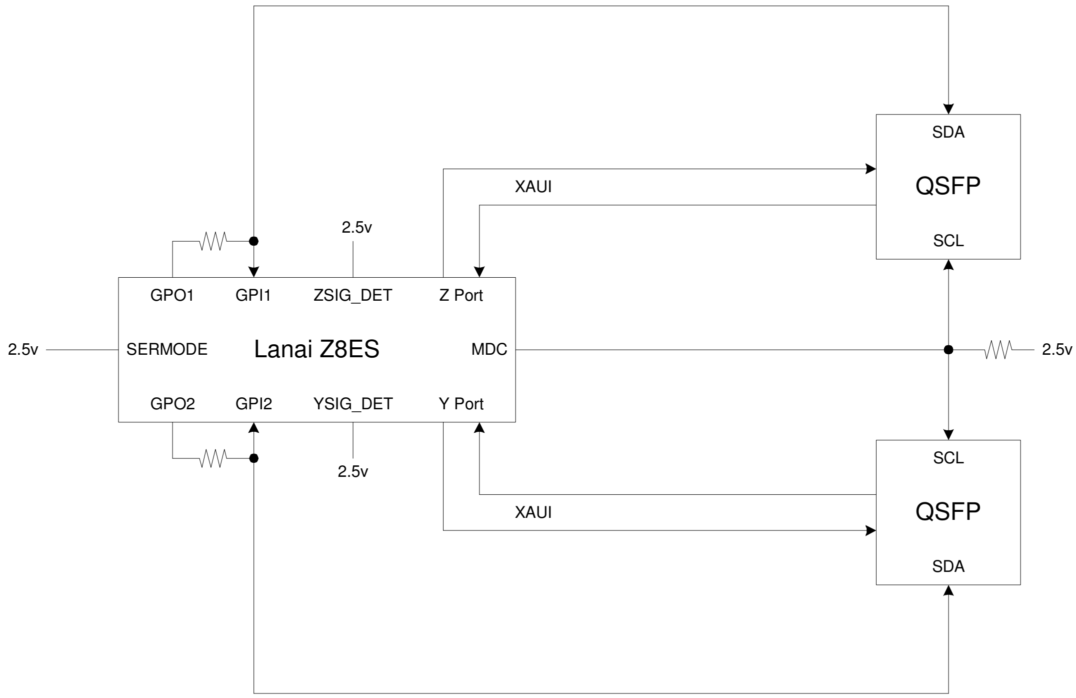
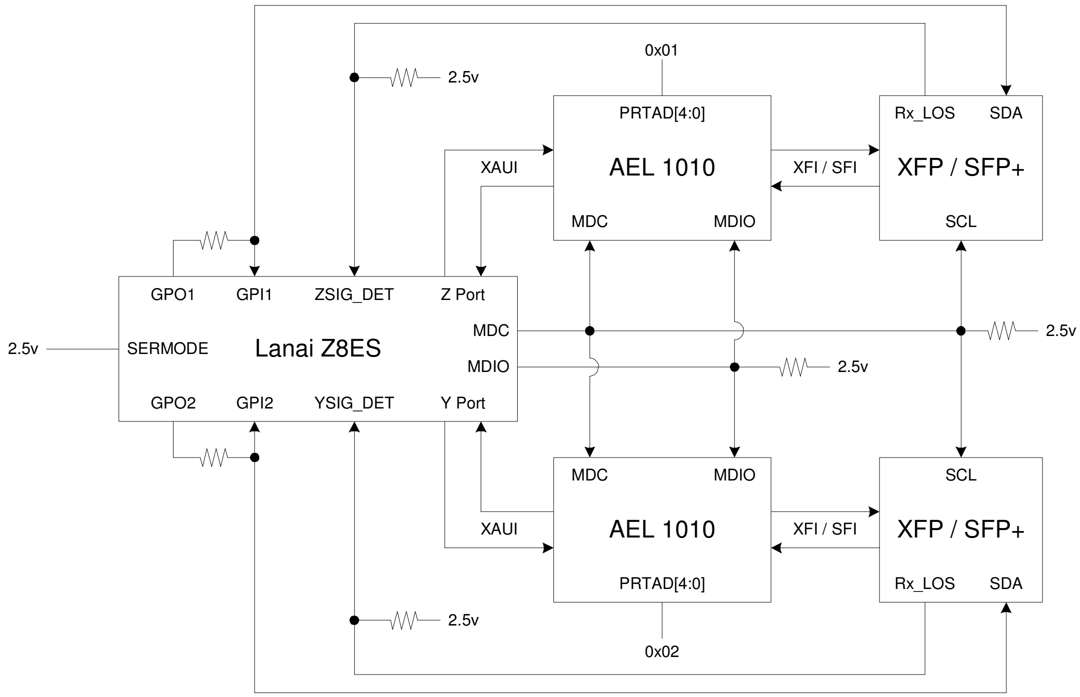


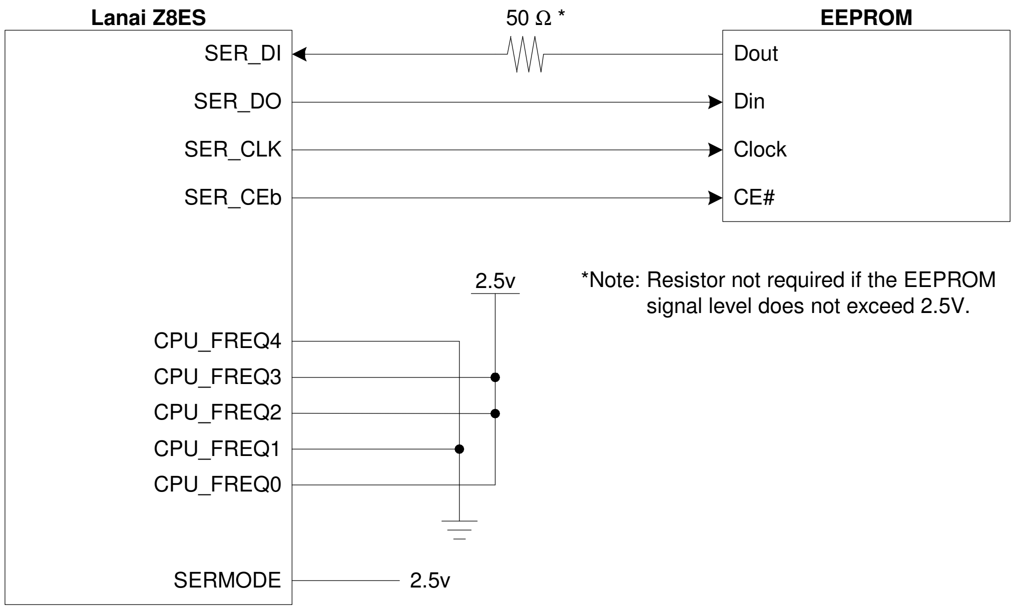
Figure 3-14: MDIO and I²C Interface Connections in a Dual-XFP/SFP+ Configuration



3.11 EEPROM Interface

The EEPROM interface of the Lanai Z8ES is designed to be directly connected to a Spansion *MirrorBit SPI FL* family or compatible serial flash device using the following wiring diagram. Myricom-compatible firmware requires an EEPROM of at least 1024Kx8.

Figure 3-15: Serial EEPROM Connection Diagram



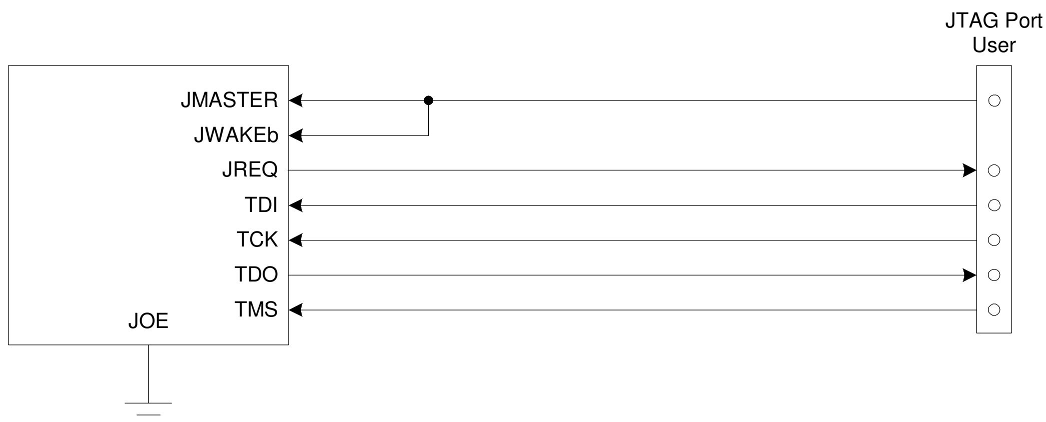
Note 1: CPU_FREQ pin-strapping value of 0x0D shown for the nominal, 338.5MHz operation. See Section 2.1.6 for details.

3.12 JTAG Interface

Although the Lanai JTAG port (TCK/TDI/TDO/TMS pins) is compatible with the JTAG standard, the scan chains do not implement boundary-scan functions and are not free to use at all times. The internal JTAG functionality is accessible via SMBus, and access via JTAG pins is deprecated; only one of these mechanisms may be used at any point in time.

If use of JTAG pins is required, the JTAG Port User must arbitrate for access to internal JTAG functionality with the Lanai CPU as illustrated below. The Lanai CPU requests JTAG access by asserting JREQ, and waits for the JTAG Port User to assert JMASTER (and de-assert JWAKEb) before accessing it.

Figure 3-16: JTAG Interface Connection Diagram



3.13 LED Signals

The following diagrams illustrate two common LED configuration options. The polarity of LED and ZLED/YLED pins is configurable. The diagrams depict connections when they are configured as negative outputs.

The LED2 and LED3 pins are available to use as general-purpose outputs.

Figure 3-17: LED Connection Diagram (Three LEDs Per Port Configuration Shown)

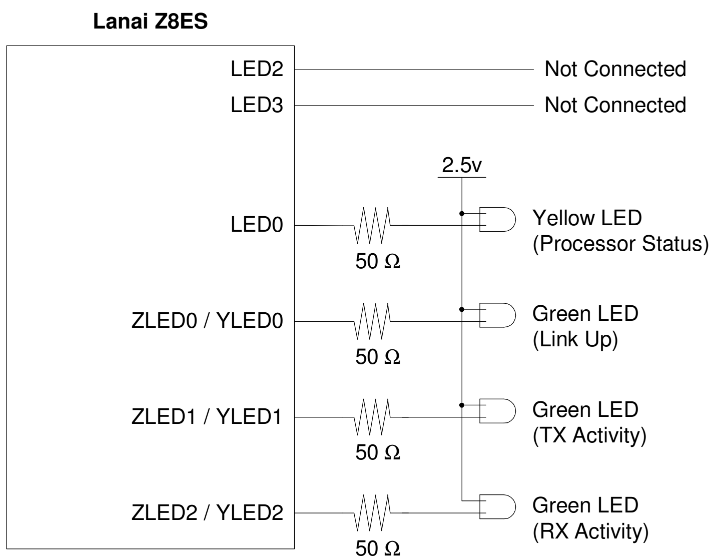
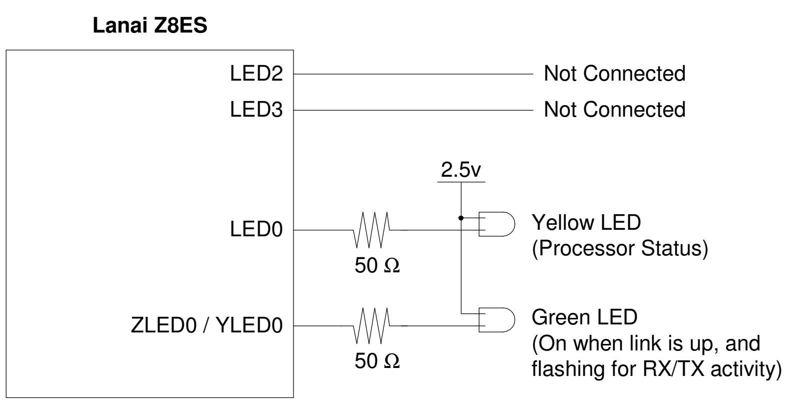


Figure 3-18: LED Connection Diagram (Single LED Per Port Configuration Shown)

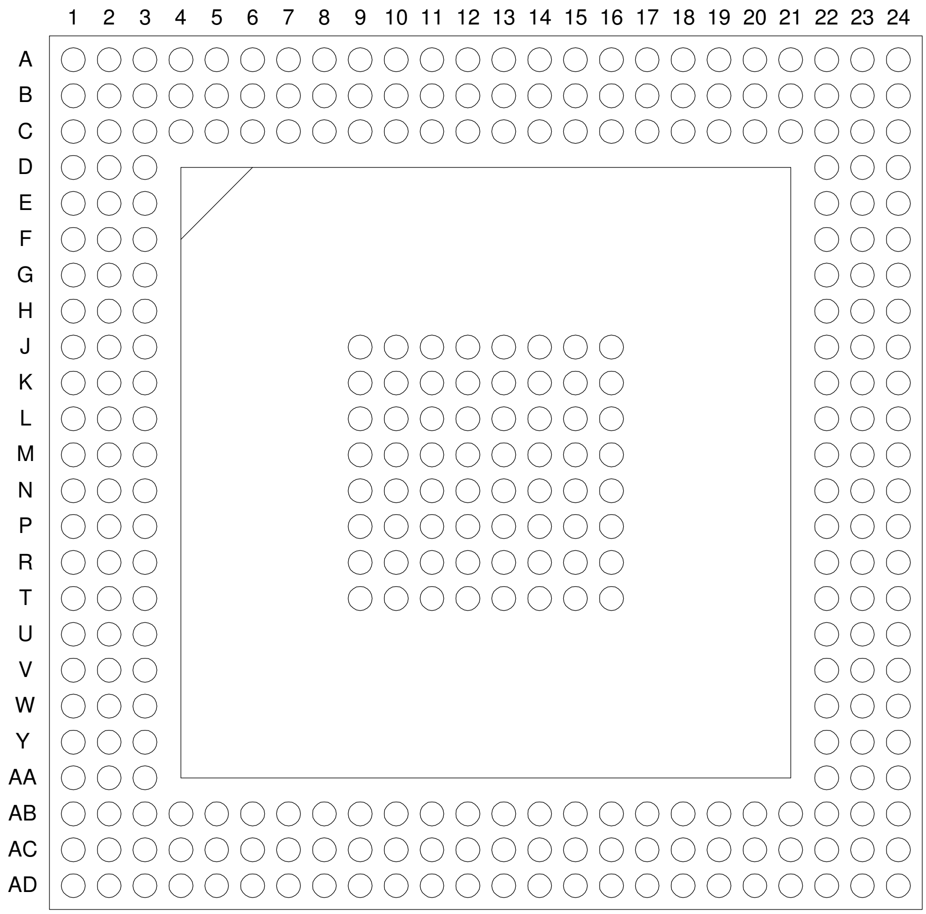


4 Package Information

4.1 Package Diagram

The Lanai Z8ES is housed in a 316-pin Flip-Chip BGA (FCBGA) chip. The pin numbering for the device is shown in the following figure.

Figure 4-1: 316-Pin FCBGA Pinout



TOP VIEW

4.2 Package Handling Information

The Lanai Z8ES has JEDEC Moisture Sensitivity Level (MSL) of 3: If out of dry pack for more than 7 days (168 hours), the chips should be baked at 125°C for 8 hours prior to soldering.

4.3 Package Dimensions

Figure 4-2: 316-Pin FCBGA Dimensions

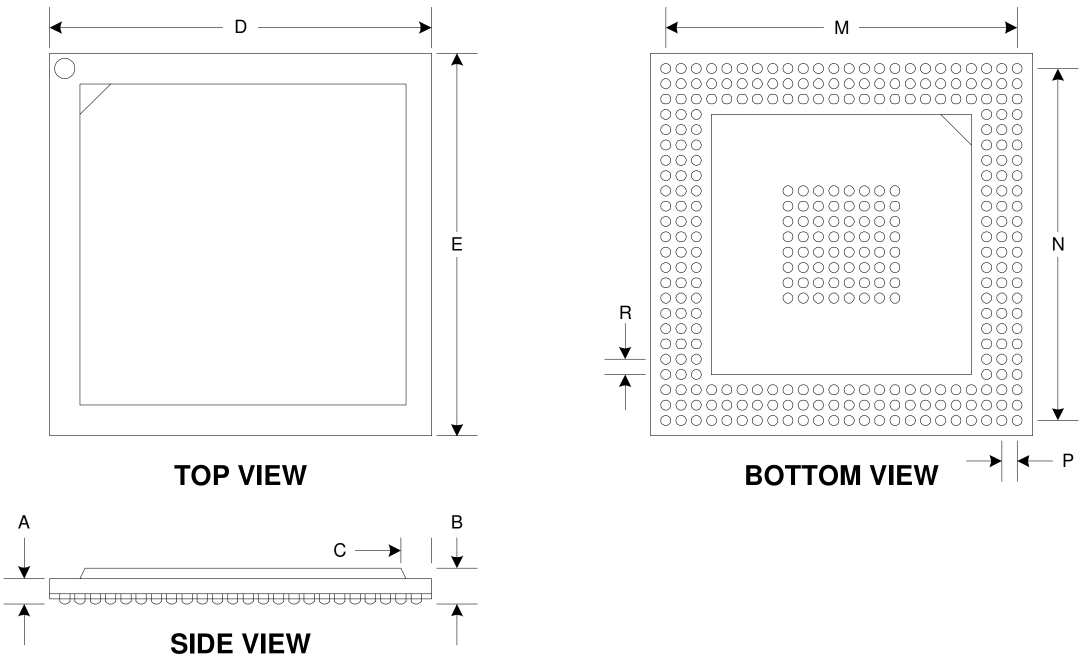


Table 4-1: 316-Pin FCBGA Dimensions

Symbol	Dimension	Value [mm]
A	Package Body Height	1.6
B	Maximum Mounted Package Height	2.5
C	Top Package Shelf	2.5
D, E	Body Size	25.0
M, N	Ball Matrix	24.0
P, R	Ball Pitch	1.00

4.4 Thermal Specifications

Table 4-2: Thermal Specifications

Symbol	Property	Air Flow [LFM]	Value [°C/W]
Θ_{CA}	Top-of-Case to Ambient Thermal Resistance	0	16.0
		100	12.4
		200	9.9
		300	8.9
		400	8.1
Θ_{JC}	Junction to Top-of-Case Thermal Resistance		2.0

Note: All Thermal Specification values are estimates. System designer must ensure that T_{CASE} limits specified in Section 3.2, Recommended Operating Conditions, are not exceeded.

Notes

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